PSMN005-75B

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 01 — 16 November 2009 Product data sheet

1. Product profile

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- High frequency computer motherboard DC-to-DC convertors
- OR-ing applicationss

1.4 Quick reference data

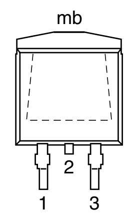
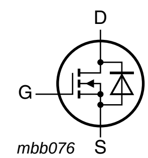
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	75	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1 and 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	230	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 75$ A; $V_{DS} = 60$ V; $T_j = 25$ °C; see Figure 11	-	50	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 9 and 10	-	4.3	5	mΩ

founded by Philips

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT404 (D2PAK)	
2	D	drain [1]		
3	S	source		
mb	D	drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

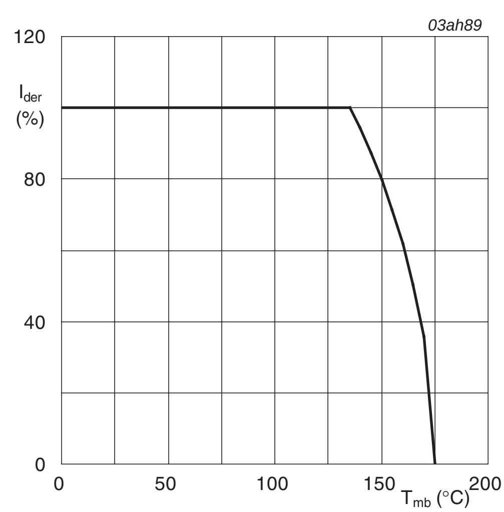
Type number	Package		
	Name	Description	Version
PSMN005-75B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

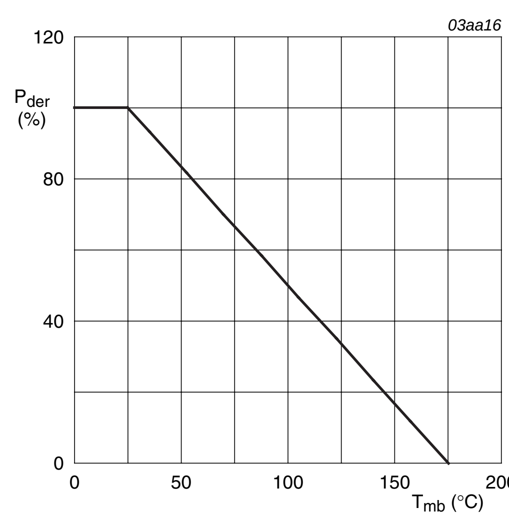
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	75	V
V_{DGR}	drain-gate voltage	$T_j \leq 175$ °C; $T_j \geq 25$ °C; R_{GS} = 20 kΩ	-	75	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	75	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1 and 3	-	75	A
I_{DM}	peak drain current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	400	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	230	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50$ µs; δ 25 %; $T_j \leq 150$ °C	-30	30	V
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	75	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C	-	400	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 75 A; V_{sup} = 15 V; unclamped; t_p = 0.1 ms; R_{GS} = 50 Ω	-	500	mJ
$I_{DS(AL)S}$	non-repetitive drain-source avalanche current	V_{GS} = 10 V; V_{sup} = 15 V; R_{GS} = 50 Ω; $T_{j(init)}$ = 25 °C; unclamped	-	75	A



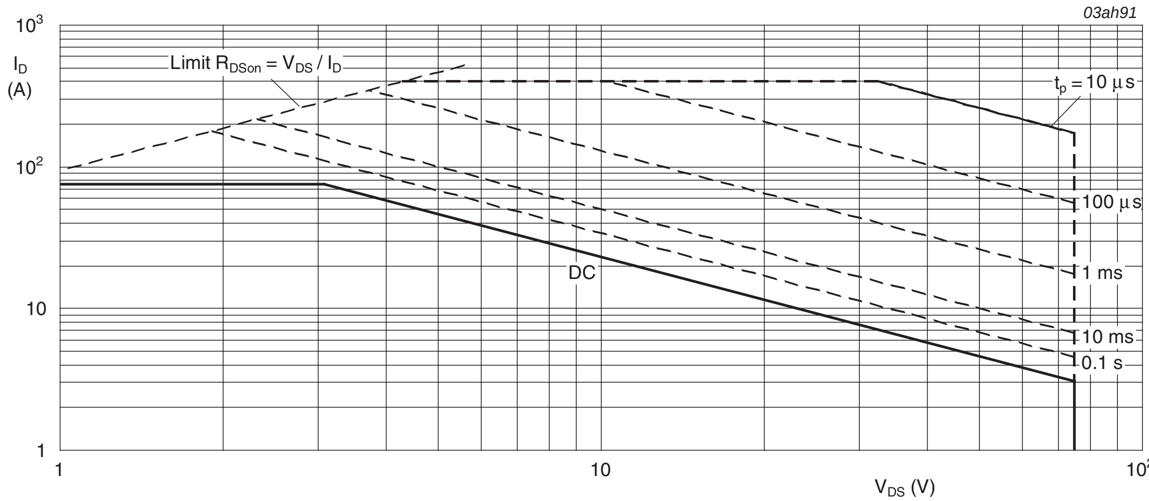
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W

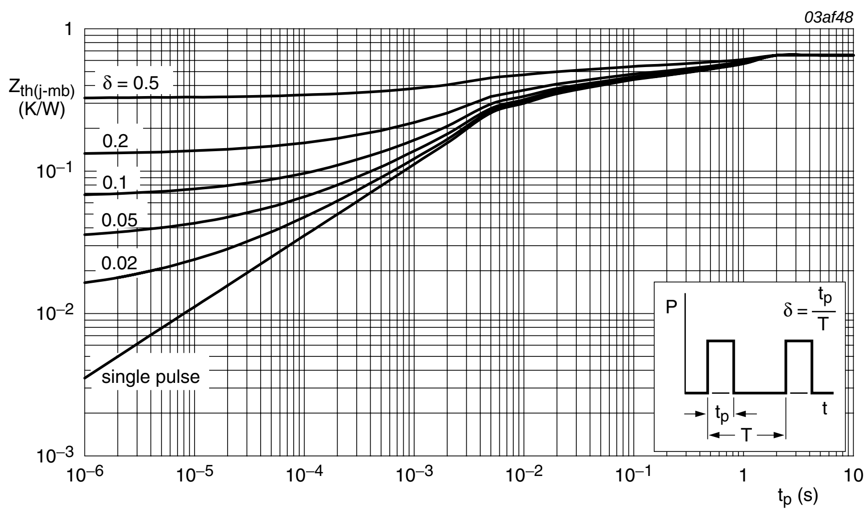
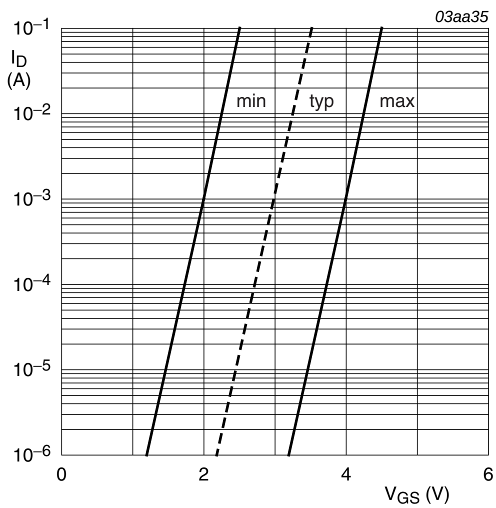


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

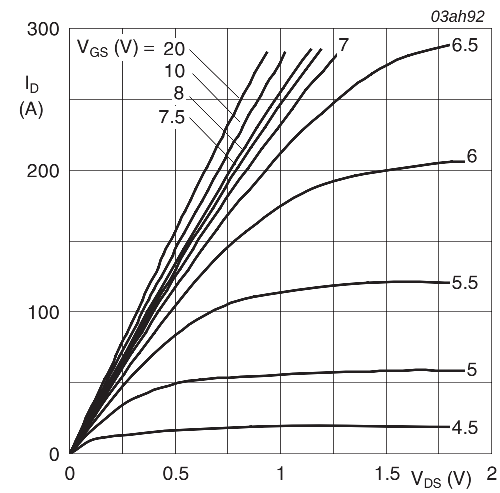
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	67	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 8	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 8	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 8	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 75 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 9 and 10	-	9.25	10.75	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 9 and 10	-	4.3	5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 75 A; V_{DS} = 60 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 11	-	165	-	nC
Q_{GS}	gate-source charge		-	32	-	nC
Q_{GD}	gate-drain charge		-	50	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	8250	-	pF
C_{oss}	output capacitance		-	920	-	pF
C_{rss}	reverse transfer capacitance		-	470	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 1.25 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	37	-	ns
t_r	rise time		-	73	-	ns
$t_{d(off)}$	turn-off delay time		-	144	-	ns
t_f	fall time		-	74	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 13	-	0.8	1.2	V



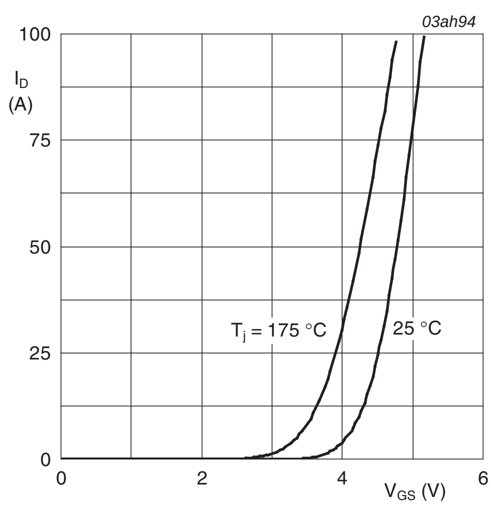
$T_j = 25\,°C; V_{DS} = 5V$

Fig 5. Sub-threshold drain current as a function of gate-source voltage



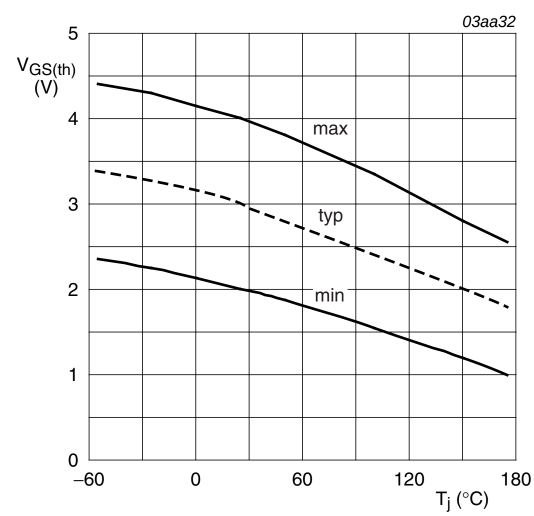
$T_j = 25°C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



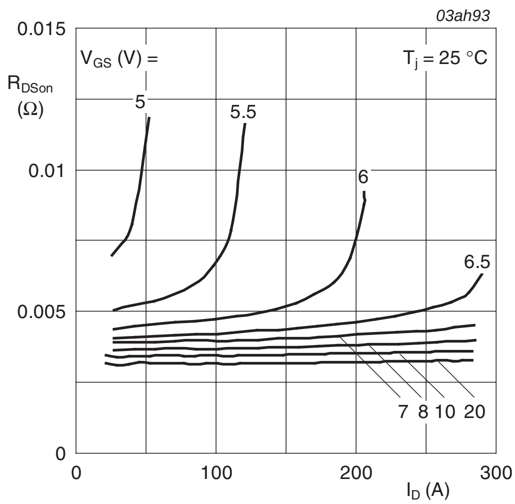
$T_j = 25°C$ and $175°C; V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



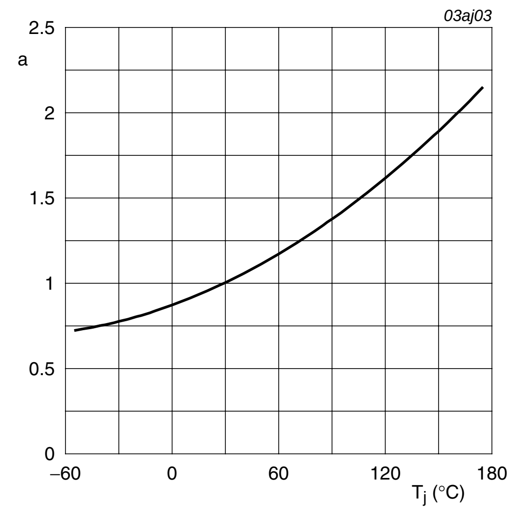
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



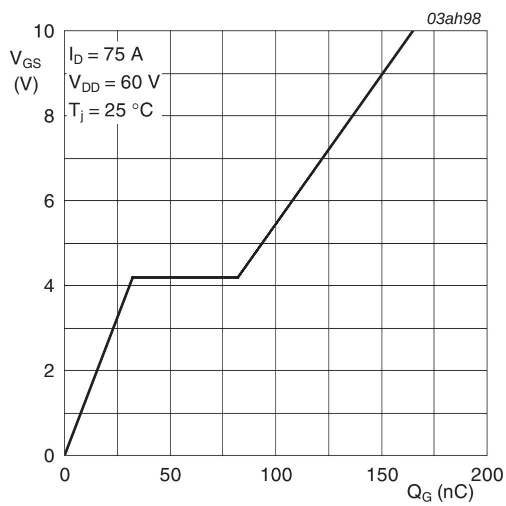
$$T_j = 25°C$$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



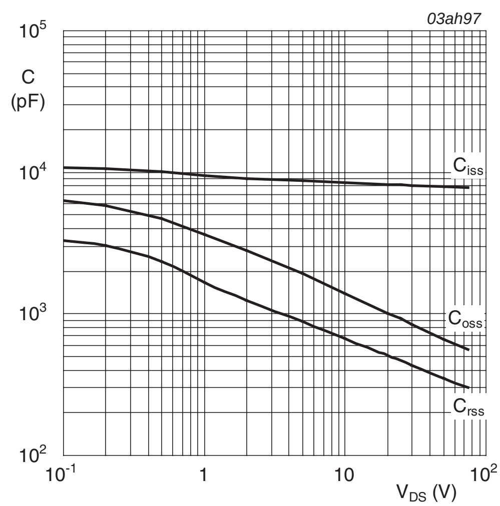
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



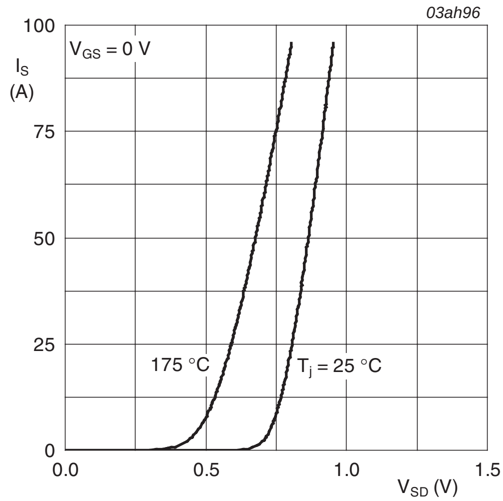
$$I_D = 75\ A; V_{DD} = 60\ V; T_j = 25\ °C$$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

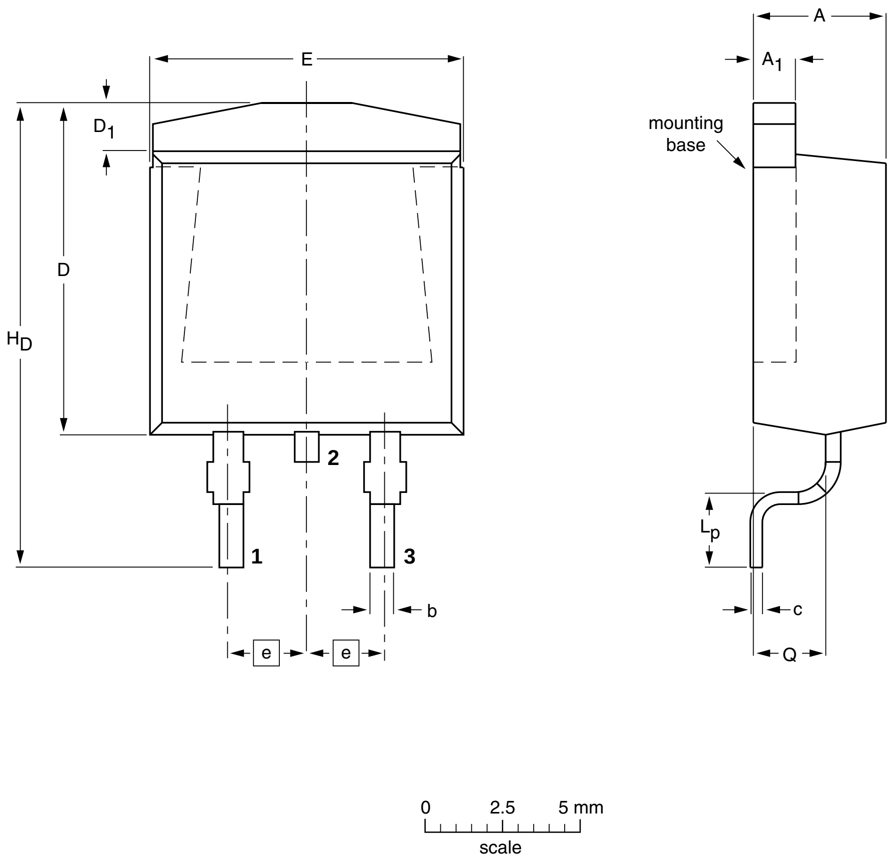


$T_j = 25°C$ and $175°C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 14. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN005-75B_1	20091116	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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